Abstract of the Disclosure

A test apparatus includes one handler connected to a tester and one test board divided into two or more sites or two or more test boards. Since only the sites on the test board (or test boards) need be duplicated, rather than the loading lanes or sorters of the handler, the test apparatus can be conveniently compact. Further, while testing semiconductor devices on one site or one test board, semiconductor devices in another site or on another test board can be sorted according to the test result. This enables the reduction or elimination of tester idle time to optimize the efficiency of the test apparatus.